Assignment 4. Solution:

Consider the following code sequence executing on a **dual-issue** CPU using **Tomasulo's** algorithm with **Reorder Buffer.**

```
Loop: L.D    F0, 0(R1)
      DIV.D  F4, F2, F0
      DADDI  R1, #-16
      S.D    F4, 8(R1)
      ADD.D  F2, #1
      BNEZ   R1, Loop
```

Assume the following

1. The architecture has one FP adder, one FP Divider, two integer units (one for integer operations and the other for address calculation) and one unit for branch condition evaluation.
2. You have unlimited reservation stations.
3. Assume that execution of the DIV.D instruction requires 8 clock cycles, ADD.D requires 4 clock cycles, while DADDI requires 3 clock cycles. All loads and stores require 2 clock cycles.
4. Assume the ability of dual-commit and dual write to CDB.
5. BNE resolved in the EX stage.
6. Assume perfect branch prediction.

Fill the following table entering the clock cycle when the instructions issue, execute, write back, and commit.

Instruction	IS	EX		WB	CM
		begin	end		
L.D F0, 0(R1)	1	2	3	4	5
DIV.D F4, F2, F0	1	5	12	13	14
DADDI R1, #-16	2	3	5	6	14
S.D F4, 8(R1)	2	14	15	-	16
ADD.D F2, #1	3	4	7	8	16
BNEZ R1, Loop	3	4	7	-	-
L.D F0, 0(R1)	4	7	8	9	17
DIV.D F4, F2, F0	4	13	20	21	22
DADDI R1, #-16	5	7	9	10	22
S.D F4, 8(R1)	6	22	25	-	26
ADD.D F2, #1	5	9	12	13	26
BNEZ R1, Loop	6	7	11	-	-

Note: RAW dependences are marked with similar colors.